

10/561632

LAP9 Rec'd PCT/PTO 19 DEC 2009

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO FORM 1449	Atty. Docket No. 10191/4152	Serial No. To Be Assigned
	Applicant(s) WEISS et al	
	Filing Date Herewith	Group To Be Assigned

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
APL	4,807,183*	Feb. 21, 1989	NISHIZAWA et al.			
APL	5,056,014*	Oct. 8, 1991	James L. BURROWS			
APL	5,448,496*	Sep. 5, 1995	BUTTS et al.			

* Copy of reference is not enclosed because reference is cited in Search Report (copy of reference provided by International Searching Authority)

FOREIGN PATENT DOCUMENTS

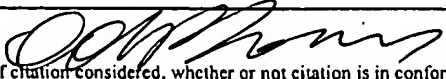
EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
APL	01 31516*	May 3, 2001	PCT				
APL	0 919 938*	Jun. 2, 1999	Europe				
APL	0 651 343*	May 3, 1995	Europe				

* Copy of reference is not enclosed because reference is cited in Search Report (copy of reference provided by International Searching Authority).

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	M. W. Rohrer, <i>AutoMod Tutorial Simulation Package</i> , Simulation Conference, IEEE Proceedings, Orlando, FL, Dec. 2000, pgs. 170-6.*
	Denielsson et al., <i>Validation, Off-Line Programming and Optimisation of Industrial Control Logic</i> , Mechatronics, Pergamon Press, Oxford, Great Britain, July 2003, Vol. 13, No. 6, pgs. 573-81.*
	Son et al., <i>Automatic Simulation Model Generation for Simulation-Based Real-Time Shop Floor Control</i> , Computers in Industry, Elsevier Science Publishers, Amsterdam, NL, July 2001, Vol. 45, No. 3, pgs. 291-308.*
	Radhakrishnan et al., <i>External Adjustment of Runtime Parameters in Time Warp Synchronized parallel Simulators</i> , Parallel Processing Symposium, IEEE Comput. Soc., CA, Apr. 1, 1997, pgs. 260-6, 303.*
	M. Buus, <i>Future Directions of Dynamically Reprogrammable Systems</i> , Proceedings of the Custom Integrated Circuits Conf., 1995, May 1, 1995, Vol. 17, pgs. 487-94.*
	D. Conner, <i>Reconfigurable Logic</i> , EDN Electrical Design News, Cahners Publishing Co., Newton, MA, March 28, 1996, Vol. 41, No. 7, pgs. 53-6, 58, 60.*

* Copy of reference is not enclosed because reference is cited in Search Report (copy of reference provided by International Searching Authority).

EXAMINER	DATE CONSIDERED
	07/26/2009
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	